Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	90	(709/211).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 17:03
S2	73	S1 and @ad < "20021127"	USPAT	OR	OFF	2005/03/21 09:14
S3	85	S1 and @ad < "20021127"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:30
S4	1895803	l	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:15
S5	33	S3 and ((slave adj1 port) or (master adj1 port) or rom or (flash adj1 memory) or usb or (usb adj1 ((on-the-go)or otg)) or (usb adj1 mass adj1 storage adj1 class adj1 ((bulk-only) or (bulk adj1 only)) adj1 transport) or (non-volatile adj1 memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:33
S6	0	(portable adj1 storage same (master or slave)) and S3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:31
S7	0	((portable adj1 storage) same (master or slave)) and S3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:33
S8	769	(709/208-211).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:33
S9	318	S8 and ((slave adj1 port) or (master adj1 port) or rom or (flash adj1 memory) or usb or (usb adj1 ((on-the-go)or otg)) or (usb adj1 mass adj1 storage adj1 class adj1 ((bulk-only) or (bulk adj1 only)) adj1 transport) or (non-volatile adj1 memory))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:34
S10	318	S9 and ad@ < "20021127"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:34
S11	1	S10 and ((portable adj1 storage) same (slave or master))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:35

S12	121	S10 and (master with slave)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:36
S13	1	(portable adj1 storage) and S12	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 09:36
S14	108	S12 and @ad < "20021127"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 10:36
S15	43160	master with slave	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 10:36
S16	59	(portable adj1 storage) and S15	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:04
S17	157	(709/253).CCLS.	USPAT	OR	OFF	2005/03/21 11:08
S18	0	S16 and S17	USPAT	OR	OFF	2005/03/21 10:37
S19	109	(master adj1 port) same (slave adj1 port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:05
S20	3	(serial adj1 bus adj1 interface) and S19	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:07
S21	0	S17 and S19	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:08
S22	22	(master with slave) and S17	USPAT	OR	OFF	2005/03/21 11:20
S23	0	((extended or portable) adj1 storage) and S22	USPAT	OR	OFF	2005/03/21 11:20
S24	0	((extended or portable) adj1 storage) and S17	USPAT	OR	OFF	2005/03/21 11:20
S25	0	((extended or portable) adj1 storage) and S17	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:21
S26	71	((extended or portable) adj1 storage) and S15	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:21

S27	60	S26 and @ad < "20021127"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 12:58
S28	33	(master same slave) and S3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 11:31
S29	10	(US-20040059923-$ or US-20040030821-$ or US-20040029407-$ or US-20020194415-$ or US-20020029303-$).did. or (US-6823411-$ or US-6779068-$ or US-6574696-$ or US-6195687-$ or US-6192392-$).did.	US-PGPUB; USPAT	OR	OFF	2005/03/21 12:53
S30	50	("5772512" "6131141" "5805842" "6016518" "5765024" "5838993" "5875351" "5065360" RE37652 "5757642" "5649233" "5732268" "6179492" "6449696" "5784581" "5602684" "5237670" "5313594" "5444858" "5577229" "5586299" "5581741" "6200289" "6230215" "5894560" "6327579" "6411943" "6553432" "6774604" "5878271" "5915100" "6270415" "5850338" "4961131" "5513334" "5551006" "5768557" "5893141" "6247088" "5831861" "5758171" "5876218" "6190182" "6061232" "5761454" "5931902" "6067618" "5210860" "5249279" "5440716").pn.	US-PGPUB; USPAT	OR	OFF	2005/03/21 12:54
S31	48	("5592648" "5771354" "5901228" "5909691" "6014651" "6505268" "5920695" "6249831" "5421014" "5657455" "5978863" "5991861" "6014726" "6118612" "6163833" "6813688" "5717930" "5978590" "6223229" "6223229" "5694600" "6061822" "6061822" "6208999" "6477624" "6598131" "4972368" "6292863" "6579185" "6722989" "6811444" "5517626" "5263172" "5268898" "5530888" "6665757" "6728534" "6125409" "5627524" "5925114" "6809631" "4907146" "5952733" "5442789" "5448742" "5467295" "5577214" "5740376" "5752075" "5887194").pn.	US-PGPUB; USPAT	OR	OFF	2005/03/21 12:53
S32	43	(master same slave) and S30	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 12:59

S33	37	(master same slave) and S31	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 12:59
S34	36	storage and S32	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 12:59
S35	26	storage and S33	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:26
S36	469	(710/110).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:52
S37	0	((portable or remote) adj1 storage) and S36	USPAT	OR	OFF	2005/03/21 13:53
S38	0	((portable or remote) adj1 storage) and S36	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:53
S39	307	(master with slave) and S36	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:55
S40	17009	connect$3 same (master with slave)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:56
S41	214	S39 and S40	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 13:56
S42	200	S41 and @ad < "20021127"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 16:06
S43	155709	intermediate with (device or storage or system or rom)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 16:08
S44	8	(mater with slave) and S43	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 16:35
S45	7	S1 and S43	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 16:23

S46	9	(mater same slave) and S43	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 16:35
S47	0	("storagesame((slaveadj1port)or(masteradj1port)or(flashadj1memory))").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 17:04
S48	10774	storage same (((master or slave) adj1 port) or (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:05
S49	7293	storage with (((master near10 slave) adj1 port) or (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:06
S50	0	storage with (((master near10 slave) adj1 port) near10 (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:06
S51	0	storage with (((master near10 slave) adj1 port) with (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:06
S52	0	storage same (((master near10 slave) adj1 port) with (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:06
S53	7293	storage with (((master near10 slave) adj1 port) or (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:06
S54	7293	storage with (((master near5 slave) adj1 port) or (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:07
S55	7293	storage with (((master near3 slave) adj1 port) or (flash adj1 memory))	USPAT	OR	OFF	2005/03/21 17:07
S56	22	((master with slave) adj1 (device or cpu or computer)) and S55	USPAT	OR	OFF	2005/03/21 17:18
S57	1065	(709/208-212).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/21 17:19
S58	1065	(709/208-212).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/21 17:19
S59	12	(master or primary) with (slave or secondary) with access$5 with (flash adj memory)	USPAT	OR	OFF	2005/03/21 17:21
S60	12	S59 and @ad<"20021127"	USPAT	OR	OFF	2005/03/21 17:20
S61	22	(master or primary) with (slave or secondary) with access$5 with (flash adj memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/21 17:22

S62	17	S61 and @ad<"20021127"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/21 17:22
S63	22	(master or primary) with (slave or secondary) with access$5 with (flash adj memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:17
S64	22	S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:24
S65	94	server with (intermedia$2 adj1 storage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:24
S66	52	client and S65	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:31
S67	313	(709/212).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/22 09:44
S68	6	((master or slave) with (connect$3 with storage)) and S67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:32
S69	2	((portable or expan$4) adj1 storage) and S67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:37
S70	127	((master or primary or server) with (slave or secondary or client)) and S67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:44
S71	6	unidirectional and S70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:38

S72	270	(master or storage or slave) and S67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 09:45
S73	1498	(710/313,74,300,110).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/22 11:54
S74	462	(master same slave) and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 11:55
S75	445	(master with slave) and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 11:55
S76	44	((flash adj1 memory) or (non-volatile adj1 memory)) and S75	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:59
S77	1	((slave adj1 port) same (master adj1 port)) and S76	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 11:56
S78	172	((extended or external or portable) with storage) and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:01
S79	47	((extended or external or portable) adj1 storage) and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:34
S80	389	(710/74).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/22 13:35
S81	289	((master or primary or first) with (slave or secondary or second)) and S80	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:36

S82	68	((flash adj1 memory) or (non-volatile adj1 memory)) and S81	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:37
S83	0	"49425519"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:59
S84	23	"4942519"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 13:59
S85	10612	(711/136-164).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/22 14:08
S86	1	((master with slave) same ((external or portable or extended) adj1 storage)) and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 14:10
S87	1	((master same slave) same ((external or portable or extended) adj1 storage)) and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 14:10
S88	13	((master same slave) same ((external or portable or extended) with storage)) and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/22 14:11
S89	3	(usb adj1 mass adj1 storage adj1 class adj1 bulk-only adj1 transport)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:05
S90	58	(usb adj1 on-the-go)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:22
S91	3923	portable adj1 storage	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:24
S92	2	S90 and S91	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:23

S93	11	(intermedia$2 adj1 storage) and S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:24
S94	12	(intermedia$2 with storage) and S90	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:24
S95	59	(master with slave) and S91	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/03/22 15:25
S96	3	"6633933"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 09:47
S97	1	(mass adj1 storage adj1 class) and S96	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:23
S98	8365	((master or slave) same ((external or portable or removable or interface or port) near10 (storage or memory or (disk adj1 extender) or hub)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:28
S99	4850	((master or slave) with ((external or portable or removable or interface or port) near10 (storage or memory or (disk adj1 extender) or hub)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:28
S100	6046	((master or slave) with ((external or portable or removable or interface or port) with (storage or memory or (disk adj1 extender) or hub)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:29
S101	3503	((master or slave) with ((external or portable or removable or interface or port) near5 (storage or memory or (disk adj1 extender) or hub)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:29
S102	1738	(prevent$3 or prohibit$3) and S101	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:29
S103	458	(usb or (universal adj1 serial adj1 bus) or (non-volatile adj1 memory) or (flash adj1 memory)) and S102	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:31

S104	370	S103 and @ad < "20021127"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:31
S105	304	S103 and @ad < "20020101"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 10:32
S106	12	"6108730"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 14:05
S107	18498	(external or portable or removable) with ((flash adj1 memory) or (non-volatile adj1 memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 14:06
S108	4908	(external or portable or removable) near3 ((flash adj1 memory) or (non-volatile adj1 memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 14:07
S109	248	(master with slave) and S108	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 16:55
S110	3	"6438683"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 16:17
S111	91	(709/211).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 16:56
S112	45	(external or portable or removable) and S111	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/24 16:56

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File 348:EUROPEAN PATENTS 1978-2005/Feb W04
         (c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050317,UT=20050310
         (c) 2005 WIPO/Univentio
File 324:German Patents Fulltext 1967-200510
         (c) 2005 Univentio

Set     Items   Description
S1    2086848   MASTER OR PRIMARY OR LEAD OR PRIME OR ALPHA OR FOREMOST OR
             ADMINISTRAT? OR MAIN OR PRINCIPAL OR LEADER OR PRIMAL OR CHIEF
              OR CENTRAL
S2     295740   HUB OR MAINFRAME? OR MAIN()FRAME? ? OR HOST
S3      82244   SERVER? OR MAILSERVER? OR MULTISERVER? OR WEBSERVER? OR PR-
             OXYSERVER? OR MINISERVER? OR CLIENTSERVER? OR PRINTSERVER? OR
             FILESERVER? OR HTTPSERVER?
S4     723245   SLAVE? ? OR CLIENT? ? OR SECONDARY OR NODE OR NODES OR SUB-
             NODE? ? OR THREAD? ?
S5      49532   NVM OR NVMS OR E2PROM? OR EEPROM? OR EAROM? OR EPROM? OR E-
             APROM? OR PROM OR PROMS OR FPROM? OR NVRAM? OR NVS
S6     160032   ROM OR ROMS
S7      20767   FLASH(1W)(MEMORY? OR MEMORIES OR STORAGE OR RAM OR RAMS)
S8     913208   MEMORY? OR MEMORIES OR STORAGE
S9      11780   (PROGRAMMAB? OR PROGRAMAB?)()(READONLY OR READ()ONLY)(1W)S8
S10      1376   (NV OR OPTICAL OR NONVOLATILE OR NON()(VOLATILE OR ERASAB?
             OR ERASEAB?))(1W)(S6 OR S9)
S11       156   (CORE OR BUBBLE OR MAGNETIC OR MAGNETO?)(1W)(S6 OR S9)
S12      1200   (NONERASEAB? OR NONERASAB? OR PERMANENT)(1W)(S6 OR S9)
S13    136075   UD OR UNIDIRECTION? OR ONEDIRECTION? OR MONODIRECTION? OR -
             (ONE OR SINGLE OR SINGULAR)(1W)DIRECTION?
S14    122290   S1(1W)(COMPUTER? ? OR UNIT OR UNITS OR TERMINAL? ? OR STAT-
             ION? ? OR DEVICE? ? OR APPLIANCE? OR PC OR PCS OR MICROCOMPUT?
              OR MICROPROCESS?)
S15     18203   S1(1W)(PROCESS?R? ? OR PCU OR PUCS OR WORKSTATION? OR CPU -
             OR CPUS)
S16       418   S14:S15(20N)S13
S17        46   S16(20N)(S5:S7 OR S9:S12)
S18      6155   IC='G06F-015/16':IC='G06F-015/167'
S19       854   IC='G06F-013/14'
S20         0   S17 AND S18:S19
S21         0   S17(20N)S4
S22        46   IDPAT S17 (sorted in duplicate/non-duplicate order)
S23        46   IDPAT S17 (primary/non-duplicate records only)
S24      1471   S2:S3(20N)S13
S25         2   S24(20N)(S5:S7 OR S9:S12)
S26         2   S25 NOT S23
S27     53009   (S2:S3 OR S14:S15)(20N)S4
S28      1310   S27(20N)(S5:S7 OR S9:S12)
S29        48   S28 AND S18:S19
S30        48   S29 NOT (S23 OR S26)
S31        48   IDPAT (sorted in duplicate/non-duplicate order)
S32        48   IDPAT (primary/non-duplicate records only)

 32/5,K/3     (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00536789
A user configurable logic device method and arrangement.
Methode und Anordnung fur eine vom Benutzer konfigurierbare logische
    Einheit.
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Methode et agencement d'un appareil logique configurable par l'utilisateur.

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PATENT (CC, No, Kind, Date): EP 499418 A2 920819 (Basic)
EP 499418 A3 940720
APPLICATION (CC, No, Date): EP 92301053 920207;
PRIORITY (CC, No, Date): GB 9103037 910213
DESIGNATED STATES: BE; DE; DK; ES; FR; GR; IT; LU; NL; PT; SE
INTERNATIONAL PATENT CLASS: **G06F-015/16**

ABSTRACT EP 499418 A2

A User Configurable Logic Device is a digital integrated circuit whose function may be tailed or adapted by the user.

A method of configuring an arrangement of user configurable logic devices including a **lead device** and one or more **slave** devices and a **PROM** comprising the step of loading into the **lead device** a configuration from the **PROM** including an external interface to the lead device. (see image in original document)

ABSTRACT WORD COUNT: 73

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	920819 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	940720 A3	Separate publication of the European or International search report
Examination:	950315 A2	Date of filing of request for examination: 950105
Withdrawal:	950503 A2	Date on which the European patent application was withdrawn: 950304

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	235
SPEC A	(English)	EPABF1	1059
Total word count - document A			1294
Total word count - document B			0
Total word count - documents A + B			1294

INTERNATIONAL PATENT CLASS: **G06F-015/16**

...ABSTRACT the user.

A method of configuring an arrangement of user configurable logic devices including a **lead device** and one or more **slave** devices and a **PROM** comprising the step of loading into the **lead device** a configuration from the **PROM** including an external interface to the lead device. (see image in original document)

...SPECIFICATION is provided a method of configuring an arrangement of user configurable logic devices including a **lead device** and one or more

slave devices and a **PROM** comprising the step of loading into the **lead device** a configuration from the **PROM** said configuration including an external interface to the lead device.

There is further provided a method as above including the step of down-loading an alternative configuration to the **slave** devices by way of the interface.

Also there is provided an arrangement of user configurable logic devices including a **lead device** and one or more **slave** devices, and a **PROM** , wherein the **PROM** is programmed to configure the arrangement to provide an external interface to the **lead device** .

Reference will now be made to arrangements using a particular form of User Configurable Logic...

...CLAIMS A2

1. A method of configuring an arrangement of user configurable logic devices including a **lead device** and one or more **slave** devices and a **PROM** comprising the step of loading into the **lead device** a configuration from the **PROM** said configuration including an external interface to the **lead device** .
2. A method as claimed in Claim 1 further including the step of down-loading an alternative configuration to the **slave** devices by way of the interface under the control of the **lead device** .
3. A method as claimed in Claim 2 wherein the **slave** devices are configured by a personal computer connected to the interface.
4. A method as...

...slave devices under control from the interface and configuring them from information stored in the **PROM** .

8. An arrangement of user configurable logic devices including a **lead device** and one or more **slave** devices, and a **PROM** , wherein the **PROM** is programmed to configure the arrangement to provide an external interface to the **lead device** .

32/5,K/26 (Item 26 from file: 349)

00935960 **Image available**

ETHERNET ADDRESSING VIA PHYSICAL LOCATION FOR MASSIVELY PARALLEL SYSTEMS
ADDRESSAGE ETHERNET EN FONCTION D'UN EMPLACEMENT PHYSIQUE POUR SYSTEMES MASSIVEMENT PARALLELES

Patent Applicant/Inventor:
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Legal Representative:
GROLZ Edward W (et al) (agent), Scully, Scott, Murphy & Presser, 400 Garden City Plaza, Garden City, NY 11530, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200269096 A2-A3 20020906 (WO 0269096)
Application: WO 2002US5570 20020225 (PCT/WO US0205570)
Priority Application: US 2001271124 20010224

Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI
SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-015/16**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 3343

English Abstract
In a massively parallel system, a method and apparatus for uniquely assigning a MAC address(400) to a device encodes the MAC address with a physical location of the device(410). The method and apparatus include configuring device interconnections of the parallel system with physical topological information such as a rack number, a midplane number, a card number, and a chip number. A device or node with a physical location encoded MAC address may then be interrogated by location for test, diagnostic, and program loading purposes.

French Abstract
L'invention concerne un systeme massivement parallele, dans lequel un procede et un appareil destines a assigner une adresse MAC unique a un dispositif, codent l'adresse MAC en fonction d'un emplacement physique du dispositif. Le procede et l'appareil permettent de configurer les interconnections du dispositif du systeme parallele avec des informations topologiques physiques telles que le numero de support, le numero de plaque centrale, le numero de carte, et le numero de puce. Un dispositif ou noeud avec une adresse MAC codee en fonction d'un emplacement physique peut alors etre interroge en fonction de l'emplacement a des fins d'essai, de diagnostic et de chargement de programme.

Legal Status (Type, Date, Text)
Publication 20020906 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20021017 Late publication of international search report
Republication 20021017 A3 With international search report.
Republication 20021017 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Examination 20030116 Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **G06F-015/16**
Fulltext Availability:
Detailed Description

Detailed Description
... e.g., compute nodes must connect to all flash memory address, data and control signals. **Flash memory** does not need to be JTAG-compliant for this programming method to function. The **host** computer sends commands and data to the JTAG-compliant device, e.g., any of compute **nodes** 205,

then propagates the data 1 5 to the **flash memory** for programming. In this manner, the **host** computer provides a communication link with any of the compute **nodes** 205 for accomplishing the physical location encoding of the MAC address. The JTAG capabilities of...

32/5,K/27 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00934992 **Image available**
SWITCHING SYSTEM
SYSTEME DE COMMUTATION
Patent Applicant/Assignee:
PIRUS NETWORKS, 43 Nagog Park, Acton, MA 01720-3425, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
LUKE Stanley, 105 Birch Hill Road, Stow, MA 01775, US, US (Residence), US (Nationality), (Designated only for: US)
HALL Howard, 86 Mara Lande, Groton, MA 01450, US, US (Residence), US (Nationality), (Designated only for: US)
COCHRANE Christopher, 7 New Road, Windham, NH 03087, US, US (Residence), US (Nationality), (Designated only for: US)
MERHAR Milan, 697 Boylston Street, Brookline, MA 02445, US, US (Residence), US (Nationality), (Designated only for: US)
FERRARI Stephen, 345 Commonwealth AVenue, Apt. 2, Boston, MA 02115, US, US (Residence), US (Nationality), (Designated only for: US)
CONDYLIS Mitchell, 31 Arrowwood Road, New Boston, NH 03070, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
JACOBS David (agent), Lucash, Gesmer & Updegrove, LLP, 40 Broad Street, Boston, MA 02109, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200269166 A1 20020906 (WO 0269166)
Application: WO 2001US45780 20011102 (PCT/WO US0145780)
Priority Application: US 2000245295 20001102
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-015/16**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 35116

English Abstract
A digital network comprises a plurality of data storage elements (104), at least one client (102) and a switch element (106) operable to receive access requests from the client (102) and provide access to data on the storage elements (104) in response to access requests.

French Abstract
La presente invention concerne un reseau numerique comprenant une pluralite d'elements de memorisation des donnees (104), au moins un client (102) et un element de commutation (106) pouvant se mettre en oeuvre de facon a recevoir des demandes du client (102) et fournir un acces aux elements de memorisation des donnees (104) en reaction aux demandes d'acces.

Legal Status (Type, Date, Text)
Publication 20020906 A1 With international search report.
Publication 20020906 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Examination 20030213 Request for preliminary examination prior to end of 19th month from priority date
Correction 20030417 Corrected version of Pamphlet: pages 1-111, description, replaced by new pages 1-118 (with an updated version of the pamphlet front page); pages 112-118, claims, replaced by new pages 119-125; pages 1/46-46/46, drawings, replaced by new pages 1/48-48/48; due to late transmittal by the receiving Office
Republication 20030417 A1 With international search report.

Main International Patent Class: **G06F-015/16**
Fulltext Availability:
Detailed Description

Detailed Description
... available for other clients to access.

In a similar fashion, the write performance of the **clients** can be improved by employing a Non-Volatile Ram (**NVRAM**) on the **client** lo **server** . Using the **NVRAM** , the system can reply to the local **clients** that
the write operation is complete as soon as the data is committed to the **NVRAM** cache. This is possible since the data will be preserved in the NVRAK and will...

32/5,K/45 (Item 45 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00105006
PERIPHERAL UNIT CONTROLLER
CONTROLEUR D'UNITES PERIPHERIQUES
Patent Applicant/Assignee:
WESTERN ELECTRIC CO INC,
Inventor(s):
LIRON M,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8100925 A1 19810402
Application: WO 80US1057 19800819 (PCT/WO US8001057)
Priority Application: US 7977512 19790920
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
JP DE FR GB NL
Main International Patent Class: **G06F-015/16**

International Patent Class: G11C-15:00; G06F-11:00
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 9470

English Abstract
Peripheral unit controller in a data processing system. The peripheral unit controller consists of two subprocessors (100a, 100d) whose outputs are matched. In addition, each duplicated subprocessor contains a pair of microprocessors (300, 307) whose outputs are also matched. The synchronization scheme allows each microprocessor (300, 307) to ran its own diagnostics independently, and to synchronize itself with the other microprocessor of the pair. After the synchronization occurs in both microprocessors in each of the sub-processors, the sub-processors are synchronized. Synchronization is achieved by using a real-time clock and the interrupt structure of each microprocessor.

French Abstract
Controleur d'unites peripheriques dans un systeme de traitement de donnees. Le controleur d'unites peripheriques se compose de deux sous-processeurs (100a, 100d) possedant des sorties appareillees. En outre, chaque sous-processeur duplique se compose d'une paire de microprocesseurs (300, 307) possedant aussi des sorties appareillees. Le chemin de synchronisation permet a chaque microprocesseur (300, 307) d'executer ces diagnostics de facon independante, de se synchroniser avec l'autre micro-processeur de la paire. Apres que la synchronisation a lieu dans les deux microprocesseurs dans chacun des sous-processeurs, les sous-processeurs sont synchronises. La synchronisation est obtenue en utilisant une horloge en temps reel et la structure d'interruption de chaque micro-processeur.

Main International Patent Class: **G06F-015/16**
Fulltext Availability:
  Detailed Description

Detailed Description
... 15 shown in detail in the drawings. Each microcomputer regardless of its designation contains a **master microprocessor** (**microprocessor** 300) and a **slave** microprocessor (microprocessor 307). Microprocessor 300 is described in a later section with respect to FIG, 12, 20 With **PROM** 304, master clock 301, PIC (priority interrupt circuit) 302, local RAM 305, transceivers 306, and...
?

? t23/5,k/2-3,15

23/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01433583
Hierarchical call control with selective broadcast audio messaging system
Hierarchische Rufsteuerung mit Audionachrichtensystem uber selektiven Rundfunk
Gestion d'appel hierarchique avec systeme de messagerie audio par diffusion selective
PATENT ASSIGNEE:
Siemens Information and Communication Mobile, L.L.C., (2910471), 2205 Grand Avenue Parkway, Austin, TX 78728-3811, (US), (Proprietor designated states: all)
INVENTOR:
Siemens, Gerhard, Startingweg 12, 46325 Borken, (DE)
LEGAL REPRESENTATIVE:
Allen, Derek et al (55491), Siemens Shared Services Limited, c/o Siemens AG, P.O. Box 22 16 34, 80506 Munich, (DE)
PATENT (CC, No, Kind, Date): EP 1213934 A2 020612 (Basic)
EP 1213934 A3 030312
EP 1213934 B1 050119
APPLICATION (CC, No, Date): EP 2001309827 011122;
PRIORITY (CC, No, Date): US 731330 001205
DESIGNATED STATES: DE; FR; GB; IT
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04Q-007/26
CITED PATENTS (EP B): EP 837611 A; WO 98/24218 A; US 5541980 A

ABSTRACT EP 1213934 A2
A cordless digital telephone system which allows hierarchical call control in a cordless phone system is provided.. Based upon a priority level associated with the identified phone number, a call controller unit directs the call to a selected one of a plurality of mobile units (412) in communication with the base station (402), or a group of mobile units (412), or in some cases, at a highest priority level, broadcasts the call to all mobile units (412). In those cases where the phone number is not identifiable as being associated with a particular priority, then a lowest priority is set for that call in which case a predefined message is sent to the caller and the call is dropped. In this way, since in a broadcast mode a user does not have the chance to prevent a ring an unwanted call can be diverted based upon a priority level such as, for example, a "Do not disturb" priority level for calls and broadcasts.
ABSTRACT WORD COUNT: 164
NOTE:
Figure number on first page: 4
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020612 A2 Published application without search report
Search Report: 030312 A3 Separate publication of the search report
Examination: 031105 A2 Date of request for examination: 20030904
Examination: 031119 A2 Date of dispatch of the first examination report: 20031007
Change: 040317 A2 Legal representative(s) changed 20040128
Grant: 050119 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 200224 406
CLAIMS B (English) 200503 454

CLAIMS B	(German)	200503	422
CLAIMS B	(French)	200503	494
SPEC A	(English)	200224	4579
SPEC B	(English)	200503	4543
Total word count - document A			4986
Total word count - document B			5913
Total word count - documents A + B			10899

...SPECIFICATION computers 404 of Fig. 4 is illustrated schematically in Fig. 8. Computer 800 includes a **central** processing **unit** (CPU) 802 which is coupled bidirectionally with random access memory (RAM) 804 and **unidirectionally** with read only memory (**ROM**) 806. Typically, RAM 804 is used as a "scratch pad" memory and includes programming instructions ...

...SPECIFICATION computers 404 of Fig. 4 is illustrated schematically in Fig. 8. Computer 800 includes a **central** processing **unit** (CPU) 802 which is coupled bidirectionally with random access memory (RAM) 804 and **unidirectionally** with read only memory (**ROM**) 806. Typically, RAM 804 is used as a "scratch pad" memory and includes programming instructions ...

23/5,K/3 (Item 3 from file: 348)

01132046

Unicode conversion into multiple encodings
Konversion von Unicode-Zeichen in mehrere Kodierungen
Conversion de caracteres Unicode en plusieurs codages

PATENT ASSIGNEE:
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INVENTOR:
Gonzalez, Julio A., 1270 Butterfly Drive, San Jose, CA 95120, (US)
Edberg, Peter K., 1892 Fairmont Boulevard, Eugene, Oregon 97403, (US)
LEGAL REPRESENTATIVE:
Schoppe, Fritz, Dipl.-Ing. (55463), Schoppe, Zimmermann & Stockeler Patentanwalte Postfach 71 08 67, 81458 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 989499 A2 000329 (Basic)
EP 989499 A3 011010
APPLICATION (CC, No, Date): EP 99118818 990923;
PRIORITY (CC, No, Date): US 161322 980925
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-017/22

ABSTRACT EP 989499 A2

Techniques to converting source text (e.g., Unicode text) to multiple different encodings are disclosed. The disclosed techniques operate without any font or style information that could suggest the original encoding types. For a given source text, the techniques intelligently determine which of a variety of available target encodings are most appropriate. The determination of the most appropriate target encodings is flexible enough to accommodate different criteria or tolerance levels in performing the conversion as may be desired. The conversion out of Unicode into multiple different encodings also requires the determination of where and when to switch between the available target encodings. Also disclosed is a technique to automatically identify those target encoding

that are available.
ABSTRACT WORD COUNT: 116
NOTE:
Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):
Change: 011010 A2 International Patent Classification changed: 20010824
Application: 20000329 A2 Published application without search report
Examination: 020807 A2 Date of dispatch of the first examination report: 20020620
Examination: 020515 A2 Date of request for examination: 20020304
Search Report: 011010 A3 Separate publication of the search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200013	1202
SPEC A	(English)	200013	10664
Total word count - document A			11866
Total word count - document B			0
Total word count - documents A + B			11866

...SPECIFICATION computer system 1000 in accordance with the present invention. The computer system 1000 includes a **central** processing **unit** (CPU) 1002, which CPU is coupled bidirectionally with random access memory (RAM) 1004 and **unidirectionally** with read only memory (**ROM**) 1006. Typically RAM 1004 includes programming instructions and data, including tables as described herein, in...

23/5,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00789102
Method and apparatus for generation and installation of distributed objects on a distributed object system
Verfahren und Gerat zum Erzeugen und Installieren von verteilten Objekten auf einem verteilten Objektsystem
Methode et appareil pour generer et installer des objets distribues sur un **systeme d'objets distribue**
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392732), 2550 Garcia Avenue, Mountain View, California 94043-1100, (US), (Proprietor designated states: all)
INVENTOR:
Snyder, Alan, 4160 Briarwood Way, Palo Alto, CA 94306, (US)
McChesney, Rod J., 28 Greenwood Lane, Redwood City, CA 94063, (US)
Hapner, Mark W., 595 Brooks Avenue, San Jose, CA 95125, (US)
van Hoff, Arthur A., 340 Ventura Avenue, No.19, Palo Alto, CA 94306, (US)
Balick, Maurice, 6711 Duck Lane, Fairhaven, MD 20754, (US)
Bracho, Rafael, 10461 Scenic Circle, Cupertino, CA 94306, (US)
LEGAL REPRESENTATIVE:
Browne, Robin Forsythe, Dr. (55142), Urquhart-Dykes & Lord Tower House Merrion Way, Leeds LS2 8PA, (GB)
PATENT (CC, No, Kind, Date): EP 735474 A2 961002 (Basic)
EP 735474 A3 970115
EP 735474 B1 030507
APPLICATION (CC, No, Date): EP 96301250 960223;
PRIORITY (CC, No, Date): US 414240 950331
DESIGNATED STATES: DE; FR; GB; IT; SE

INTERNATIONAL PATENT CLASS: G06F-009/46
CITED REFERENCES (EP B):
"SOMobjects Developer Toolkit Users Guide" October 1994 , IBM , ARMONK, USA XP002018414 * Chap. 4, SOM IDL and the SOM Compiler; Chap. 5, Implementing Classes in SOM * * Chap. 6, Distributed SOM (DSOM) * * page 4-33 - page 4-36 * * page 5-10 - page 5-12 * * page 5-16 - page 5-19 * * page 5-53 - page 5-56 * * page 6-31 - page 6-49 * * page 6-57 - page 6-59 * * page 6-70 - page 6-72 * * page 6-81 * * page 6-84 *
BJARNE STROUSTRUP: "The C++ programming language" 1992 , ADDISON-WESLEY , READING, MA, USA XP002018415 18712 * pp. 191-193, Section 6.3, Abstract Classes * * pp. 434-439, Section 13.3, Abstract Types, page 434 * * pp. 457-460, Section 13.8, Interface Classes, page 457, lines 1-19 * * pp. 460-465, Section 13.9, Handle classes, page 464, 2nd example *
DR. DOBB'S SPECIAL REPORT, vol. 19, no. 16, December 1994, MILLER FREEMAN, USA, pages 8-12, XP002018413 MARK BETZ: "OMG's CORBA";

ABSTRACT EP 735474 A2
A method and apparatus for installing distributed objects on a distributed object system is described. In one aspect the distributed objects include wrapper classes that inherit object attributes through an inheritance relationship with a developer-written servant class of objects, the developer-written servant classes inheriting attributes through an optional inheritance relationship with an interface class of objects. In a preferred embodiment, the wrapper classes provide an interface mechanism between the methods of the servant class of objects and the object request broker mechanism of the distributed object system. Also included is an apparatus for creating and installing the distributed object in the memory of a computer on a distributed object system. The invention further includes a mechanism for distinguishing deployed distributed objects from development distributed objects.
ABSTRACT WORD COUNT: 141
NOTE:
Figure number on first page: NONE

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	030507	B1	Granted patent
Application:	961002	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	040428	B1	No opposition filed: 20040210
Search Report:	970115	A3	Separate publication of the European or International search report
Examination:	970502	A2	Date of filing of request for examination: 970304

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200319	1756
CLAIMS B	(German)	200319	1553
CLAIMS B	(French)	200319	2089
SPEC B	(English)	200319	9812
Total word count - document A			0
Total word count - document B			15210
Total word count - documents A + B			15210

...SPECIFICATION 112 are illustrated schematically with respect to Figure 2 at 200. Each computer includes a **central** processing **unit** (CPU) 202 which CPU is coupled bidirectionally with random access memory (RAM) 204 and **unidirectionally** with read only memory (**ROM**) 206. Typically, RAM 204 includes programming instructions and data, including distributed objects and their associated...
? t23/5,k/23-24

23/5,K/23 (Item 23 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01177478 **Image available**

METHOD AND SYSTEM FOR PROVIDING MAP INFORMATION TO MOBILE DEVICE

PROCEDE ET SYSTEME PERMETTANT DE FOURNIR DES INFORMATIONS CARTOGRAPHIQUES A UN DISPOSITIF MOBILE

Patent Applicant/Assignee:
THINKWARE SYSTEMS CORPORATION, Hanmi Tower 15 F., 45 Bangi-dong, Songpa-gu, 138-050 Seoul, KR, KR (Residence), KR (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
CHOI Won Ik, #102-703, Byucksan Apartment, Jowon-dong, Jangan-gu, 440-200 Suwon-si, Kyunggi-do, KR, KR (Residence), KR (Nationality), (Designated only for: US)
KIM Byeong Moo, 304-16, Gabong 2-dong, Guro-gu, 152-092 Seoul, KR, KR (Residence), KR (Nationality), (Designated only for: US)
Legal Representative:
CHUN Sung Jin (agent), Muhann Patent & Law Firm, 5th Fl., Youngpoong Bldg., 142 Nonhyun-dong, Kangnam-gu, 135-749 Seoul, KR,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200499719 A1 20041118 (WO 0499719)
Application: WO 2003KR2218 20031022 (PCT/WO KR03002218)
Priority Application: KR 1020030029572 20030510
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G01C-021/32
International Patent Class: G01C-021/00
Publication Language: English
Filing Language: Korean
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 9417

English Abstract
The present invention relates to a method of efficiently transmitting a plurality of levels of map information to a mobile device so that a map can be magnified or reduced on the mobile device. The method for providing map information to a mobile device of the present invention, is characterized in that comprises the steps of maintaining a map information database containing a plurality of map data elements each of which is associated with coordinate information and level information; receiving a request for map information from the mobile device; searching for the map data elements associated with position information corresponding to the map information request; and transmitting the searched map data elements to the mobile device along with the display level information associated with the searched map data elements. According to the present invention, when map information is provided to a

mobile device, an amount of data to be transmitted can be minimized by dividing a map corresponding to a single area into a plurality of levels and transmitting map information data common to the respective levels in a shared manner.

French Abstract
L'invention concerne un procede permettant de transmettre efficacement plusieurs niveaux d'informations cartographiques a un dispositif mobile de facon qu'une carte puisse etre grossie ou reduite sur ce dispositif mobile. Le procede de cette invention permettant de fournir des informations cartographiques a un dispositif mobile, est caracterise en ce qu'il comprend les etapes consistant a conserver une base de donnees d'informations cartographiques contenant plusieurs elements de donnees cartographiques, chacun associe a des informations de coordonnees et des informations de niveaux, a recevoir une demande d'informations cartographiques du dispositif mobile, a rechercher les elements de donnees cartographiques associes avec des informations de position correspondant a la demande d'informations cartographiques, et a transmettre les elements de donnees cartographiques recherches au dispositif mobile avec les informations de niveau d'affichage associees aux elements de donnees cartographiques recherches. Selon cette invention, lorsque des informations cartographiques sont fournies a un dispositif mobile, la quantite de donnees devant etre transmises peut etre reduite au maximum par division d'une carte correspondant a une zone unique en plusieurs niveaux et par transmission des donnees d'informations cartographiques communes aux niveaux respectifs de facon partagee.

Legal Status (Type, Date, Text)
Publication 20041118 A1 With international search report.
Fulltext Availability:
Detailed Description

Detailed Description
... processor 901 that is connected to a main memory having a RAM 902 and a **ROM** 903. The processor 901 is also called a **central** processing **unit** (CPU). As well known in the art, the **ROM** 903 functions to transfer data and instructions **unidirectionally** to the CPU, and the RAM 902 is usually used to transfer data and instructions...

23/5,K/24 (Item 24 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00957015 **Image available**
APPARATUS AND METHOD FOR UNIFORMLY PERFORMING COMPARISON OPERATIONS ON LONG WORD OPERANDS
APPAREIL ET PROCEDE DE MISE EN OEUVRE UNIFORME D'OPERATIONS DE COMPARAISON SUR DES OPERANDES DE MOTS LONGS
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, 901 San Antonio Road, M/S: PAL01-521, Palo Alto, CA 94303, US, US (Residence), US (Nationality)
Inventor(s):
GRIESEMER Robert, 3881 Magnolia Drive, Palo Alto, CA 94303, US,
Legal Representative:
WEAVER Jeffrey K (agent), Beyer Weaver & Thomas, LLP, P.O. Box 778, Berkeley, CA 94704-0778, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200291166 A2-A3 20021114 (WO 0291166)
Application: WO 2002US13927 20020503 (PCT/WO US0213927)

Priority Application: US 2001848976 20010503
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI
SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06F-007/02
International Patent Class: G06F-009/32
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5908

English Abstract
Using a subtraction without borrow operation, the first operand lowest order word is subtracted from a second operand lowest order word. If the result of the subtracting is not zero, then a zero (Z) flag is cleared such that a Z flag status is not set. If, however, the result of the subtracting is zero, then the Z flag is set as usual. Next, a first operand next higher order word is subtracted from a second operand next higher order word using a subtraction withborrow and a sticky not Z flag (SBBZ) instruction and, based upon the subtracting, the Z flag is updated accordingly such that it represents the result of the whole multi-word subtraction until the first operand highest order word is subtracted from the second operand highest order word. The comparing of the first operand and the second operand is then based upon the Z flag status, if needed, after the subtraction of the first operand highest order word is subtracted from the second operand highest order word.

French Abstract
Selon l'invention, par utilisation d'une soustraction sans operation d'emprunt, le plus bas mot d'ordre de premier operande est soustrait d'un plus bas mot d'ordre de second operande. Si le resultat de la soustraction n'est pas egal a zero, alors un indicateur zero (Z) est efface de sorte qu'un statut indicateur Z n'est pas defini. Si, cependant, le resultat de la soustraction est egal a zero, alors l'indicateur Z est defini comme habituel. Ensuite, un plus eleve mot d'ordre de premier operande suivant est soustrait d'un plus eleve mot d'ordre de second operande suivant a l'aide d'une soustraction avec emprunt et d'une instruction d'indicateur de rappel non egal a zero (SBBZ) et, en fonction de la soustraction, l'indicateur Z est par consequent mis a jour de sorte qu'il represente le resultat de la soustraction entiere de mots multiples jusqu'a ce que le plus eleve mot d'ordre de premier operande soit soustrait du plus eleve mot d'ordre de second operande. La comparaison du premier operande et du second operande est ensuite basee sur le statut d'indicateur Z, si necessaire, apres que la soustraction du plus eleve mot d'ordre de premier operande est soustraite du plus eleve mot d'ordre de second operande.

Legal Status (Type, Date, Text)
Publication 20021114 A2 Without international search report and to be republished upon receipt of that report.
Examination 20030109 Request for preliminary examination prior to end of

19th month from priority date
Search Rpt 20031023 Late publication of international search report
Republication 20031023 A3 With international search report.

Fulltext Availability:
Detailed Description

Detailed Description
... be incorporated in standard fashion as part of RAM 336 as virtual memory. A specific **primary** storage **device** 334 such as a CD- **ROM** may also pass data **unidirectionally** to the CPUs 332.

CPUs 332 are also coupled to one or more input/output...
?

File 347:JAPIO Nov 1976-2004/Nov(Updated 050309)
(c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200519
(c) 2005 Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2005/Feb W04
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050317,UT=20050310
(c) 2005 WIPO/Univentio
File 324:German Patents Fulltext 1967-200510
(c) 2005 Univentio

Set	Items	Description
S1	2172	AU=LIN H?
S2	433	AU=FANG J?
S3	2601	S1:S2
S4	3446	PORTAB?(1W)STORAGE
S5	1	S3 AND S4

5/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016290176 **Image available**
WPI Acc No: 2004-448071/200442
XRPX Acc No: N04-354391
Portable storage **device for use with master and slave computers, has flash memory to store data in device, and slave and master ports, both connecting device to slave and master computers via serial bus interface, respectively**
Patent Assignee: YANGZHI SCI & TECHNOLOGY CO LTD (YANG-N); FANG J (FANG-I); LIN H (LINH-I)
Inventor: **FANG J** ; **LIN H**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040103163	A1	20040527	US 200265903	A	20021127	200442	B
CN 1503149	A	20040609	CN 2003123483	A	20030509	200460	

Priority Applications (No Type Date): US 200265903 A 20021127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040103163	A1		12	G06F-015/16	
CN 1503149	A			G06F-015/16	

Abstract (Basic): US 20040103163 A1
NOVELTY - The device has a flash memory for storing data in the **portable storage** device. A slave port (60) connects the portable device to a slave computer (64) through a universal serial bus interface. A master port (52) connects the **portable storage** device to a master computer (62) through the serial bus interface. An expansion port connects an external storage apparatus to the storage device.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of connecting a **portable storage** device to a master computer and a slave computer through a serial bus interface.
USE - Used for connecting a master computer and a slave computer through a serial bus interface (claimed).
ADVANTAGE - The device is capable of providing the master computer to access the data located on the **portable storage** device and the

slave computer, while at the same time preventing the slave computer to access data either on the device or the master computer.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a disk extender.

Master port (52)
Expansion slot (58)
Slave port (60)
Master computer (62)
Slave computer (64)
pp; 12 DwgNo 3/7

Technology Focus:

TECHNOLOGY FOCUS - INDUSTRIAL STANDARDS - The universal serial bus is an IEEE 1394 interface.

Title Terms: PORTABLE; STORAGE; DEVICE; MASTER; SLAVE; COMPUTER; FLASH; MEMORY; STORAGE; DATA; DEVICE; SLAVE; MASTER; PORT; CONNECT; DEVICE; SLAVE; MASTER; COMPUTER; SERIAL; BUS; INTERFACE; RESPECTIVE

Derwent Class: T01; U13; U14

International Patent Class (Main): G06F-015/16

International Patent Class (Additional): G06F-013/14

File Segment: EPI

Manual Codes (EPI/S-X): T01-C07C; T01-H01B3A; T01-H07A; T01-M02D; U13-C04D; U14-A03B7

?

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File 347:JAPIO Nov 1976-2004/Nov(Updated 050309)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200519
         (c) 2005  Thomson Derwent
File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.

Set     Items   Description
S1    2869544   MASTER OR PRIMARY OR LEAD OR PRIME OR ALPHA OR FOREMOST OR
             ADMINISTRAT? OR MAIN OR PRINCIPAL OR LEADER OR PRIMAL OR CHIEF
              OR CENTRAL
S2     216864   HUB OR MAINFRAME? OR MAIN()FRAME? ? OR HOST
S3     159192   SERVER? OR MAILSERVER? OR MULTISERVER? OR WEBSERVER? OR PR-
             OXYSERVER? OR MINISERVER? OR CLIENTSERVER? OR PRINTSERVER? OR
             FILESERVER? OR HTTPSERVER?
S4     650179   SLAVE? ? OR CLIENT? ? OR SECONDARY OR NODE OR NODES OR SUB-
             NODE? ? OR THREAD? ?
S5      27433   NVM OR NVMS OR E2PROM? OR EEPROM? OR EAROM? OR EPROM? OR E-
             APROM? OR PROM OR PROMS OR FPROM? OR NVRAM? OR NVS
S6      78295   ROM OR ROMS
S7      15503   FLASH(1W)(MEMORY? OR MEMORIES OR STORAGE OR RAM OR RAMS)
S8    1757694   MEMORY? OR MEMORIES OR STORAGE
S9       4771   (PROGRAMMAB? OR PROGRAMAB?)()(READONLY OR READ()ONLY)(1W)S8
S10       261   (NV OR OPTICAL OR NONVOLATILE OR NON()(VOLATILE OR ERASAB?
             OR ERASEAB?))(1W)(S6 OR S9)
S11        30   (CORE OR BUBBLE OR MAGNETIC OR MAGNETO?)(1W)(S6 OR S9)
S12        39   (NONERASEAB? OR NONERASAB? OR PERMANENT)(1W)(S6 OR S9)
S13     80189   UD OR UNIDIRECTION? OR ONEDIRECTION? OR MONODIRECTION? OR -
             (ONE OR SINGLE OR SINGULAR)(1W)DIRECTION?
S14    129857   S1(1W)(COMPUTER? ? OR UNIT OR UNITS OR TERMINAL? ? OR STAT-
             ION? ? OR DEVICE? ? OR APPLIANCE? OR PC OR PCS OR MICROCOMPUT?
              OR MICROPROCESS?)
S15     17292   S1(1W)(PROCESS?R? ? OR PCU OR PUCS OR WORKSTATION? OR CPU -
             OR CPUS)
S16     12243   (S1:S2 OR S14:S15) AND S13
S17        45   S16 AND (S5:S7 OR S9:S12)
S18     52822   IC='G06F-015/16':IC='G06F-015/1677'
S19     10465   IC='G06F-013/14':IC='G06F-013/144'
S20       667   MC='T01-M02D'
S21      7171   MC='T01-H01B3A'
S22         7   S20 AND S21
S23      2684   MC='T01-H07A'
S24     16003   MC='U14-A03B7'
S25         1   S20 AND S24
S26      4164   MC='T01-C07C'
S27      2684   MC='T01-H07A'
S28      5053   MC='U13-C04D'
S29         3   S17 AND (S18:S21 OR S23:S24 OR S26:S28)
S30     70589   (S2:S3 OR S14:S15) AND S4
S31       622   S30 AND (S5:S7 OR S9:S12)
S32        73   S31 AND S18:S19
S33   2374608   MASTER OR PRIMARY OR LEAD OR PRIME OR ALPHA OR FOREMOST OR
             ADMINISTRAT? OR MAIN OR PRINCIPAL OR LEADER OR PRIMAL OR CHIEF
S34     80615   S33(1W)(COMPUTER? ? OR UNIT OR UNITS OR TERMINAL? ? OR STA-
             TION? ? OR DEVICE? ? OR APPLIANCE? OR PC OR PCS OR MICROCOMPU-
             T? OR MICROPROCESS?)
S35      4258   CENTRAL()(UNIT OR UNITS)
S36     14613   CENTRAL(1W)(COMPUTER? ? OR TERMINAL? ? OR STATION? ? OR DE-
             VICE? ? OR APPLIANCE? OR PC OR PCS OR MICROCOMPUT? OR MICROPR-
```

OCESS?)
S37 1407 (S2 OR S15 OR S34:S36) AND S13
S38 23 S37 AND (S5:S7 OR S9:S12)
S39 29166 (S2 OR S15 OR S34:S36) AND S4
S40 373 S39 AND (S5:S7 OR S9:S12)
S41 47 S40 AND S18
S42 7 S40 AND S19
S43 3 S41 AND (S20:S21 OR S23:S24 OR S26:S28)
S44 10 S22 OR S25 OR S29
S45 10 IDPAT (sorted in duplicate/non-duplicate order)
S46 10 IDPAT (primary/non-duplicate records only)
S47 30 (S38 OR S42:S43) NOT S46
S48 30 IDPAT (sorted in duplicate/non-duplicate order)
S49 29 IDPAT (primary/non-duplicate records only)
S50 1092 S4(20N)(S5:S7 OR S9:S12)
S51 28 S41 AND S50
S52 26 S51 NOT (S46 OR S47)
S53 26 IDPAT (sorted in duplicate/non-duplicate order)
S54 25 IDPAT (primary/non-duplicate records only)

54/9/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

03913547 **Image available**
SELF-DIAGNOSTIC SYSTEM

PUB. NO.: 04-278647 [JP 4278647 A]
PUBLISHED: October 05, 1992 (19921005)
INVENTOR(s): NAKAGAWA TATSUHIKO
OGURA IKUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
NEC ENG LTD [329822] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-065533 [JP 9165533]
FILED: March 06, 1991 (19910306)
INTL CLASS: [5] G06F-011/22; **G06F-015/16**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1487, Vol. 17, No. 76, Pg. 2, February 16, 1993 (19930216)

ABSTRACT

PURPOSE: To ensure an effective diagnosis of a control circuit of a large scale by diagnosing all peripheral circuits provided on the **slave** processors in response to a **master processor** and informing the diagnostic results to the **master processor** .

CONSTITUTION: A **master processor** 11 detects the signal received from a self- diagnostic start switch 14 and sends a self-diagnostic request command to the **slave** processors 21 and 31 respectively. At the same time, the processor 11 checks the **ROM** 22 and 23, the RAM 23 and 33, and an input/output port, etc., of its own. Then each **slave** processor that completed the diagnosis of a fault in its circuit sends in reply the contents of the fault part to the processor 11. The processor 11 displays the received contents on a display device 15 together with its own check result.

54/9/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

02916141 **Image available**
MULTIPROCESSOR SYSTEM

PUB. NO.: 01-213741 [JP 1213741 A]
PUBLISHED: August 28, 1989 (19890828)
INVENTOR(s): TANIGUCHI EI
KURIWAKI MASASHI
APPLICANT(s): SEKISUI CHEM CO LTD [000217] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-038304 [JP 8838304]
FILED: February 19, 1988 (19880219)
INTL CLASS: [4] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 964, Vol. 13, No. 524, Pg. 79, November 22, 1989 (19891122)

ABSTRACT

PURPOSE: To considerably reduce the number of times of synchronous communication between CPUs and to improve the parallel processing capability by storing a series of commands as a new command group and successively executing this command group.

CONSTITUTION: A **master CPU** 1 writes a command for output contents to a shared memory 2 at the time of output to a display device 4. A **slave** CPU 3 reads out the command written in the shared memory 2 and performs the processing in accordance with a program in a **ROM** 5. The **master CPU** 1 transfers segment execution commands to the shared memory 2 to terminate the processing. Meanwhile, the **slave** CPU 3 receives segment execution commands by synchronous communication with the master MPU 1 and executes the first command and successively executes commands till the end of a segment. The picture on the display device 4 is switched with only one synchronous communication.
? t54/9/17,13,8

54/9/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

02716063 **Image available**
ARITHMETIC UNIT

PUB. NO.: 01-013663 [JP 1013663 A]
PUBLISHED: January 18, 1989 (19890118)
INVENTOR(s): MURATA JUNICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-170135 [JP 87170135]
FILED: July 07, 1987 (19870707)
INTL CLASS: [4] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 866, Vol. 13, No. 188, Pg. 25, May 08, 1989 (19890508)

ABSTRACT

PURPOSE: To execute an optimum control in accordance with an input signal and to execute the miniaturization and low power consumption of a circuit

by rewriting the program of a **slave** CPU during the action by the value of an inputted analog signal with a **master CPU** .
CONSTITUTION: To the program storage device of a **slave** CPU 2, an electrically rewritable **ROM** 5 is used, a program can be re-written by the instruction from a **master CPU** 1 during the action of the circuit, the program of the **slave** CPU 2 can be re-written and processed in accordance with the value of an analog signal, and even when the power source of the circuit is turned off, the program of the **slave** CPU 2 is held. The program of the **slave** CPU 2 can be re-written during the circuit action by the instruction from the **master CPU** 1 and the control in accordance with the value of the inputted analog signal can be executed.

54/9/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

03545258 **Image available**
ELECTRONIC CONTROLLER

PUB. NO.: 03-208158 [JP 3208158 A]
PUBLISHED: September 11, 1991 (19910911)
INVENTOR(s): ITO NORIFUMI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-003107 [JP 903107]
FILED: January 10, 1990 (19900110)
INTL CLASS: [5] **G06F-015/16** ; G06F-009/06; G06F-011/00
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1285, Vol. 15, No. 483, Pg. 25, December 06, 1991 (19911206)

ABSTRACT

PURPOSE: To avoid the occurrence of the abnormality of an action owing to the combination of the types of program storage means by collectively storing control program data in a master control means and a **slave** control means in single **ROM** .

CONSTITUTION: Program data for **master CPU** 20 and **slave** CPU 80 are previously stored on **ROM** 50 in prescribed address arrangement. The action of CPU 80 is prohibited immediately after power is supplied, and CPU 20 transfers program data for CPU 80, which is stored in **ROM** 50, onto a common memory means RAM 70. Then, the action of CPU 80 is allowed and CPU 80 reads data transferred on RAM 70 and executes the program. Writing can be executed on RAM 70 from CPU 80 and the area of program data and the work area of CPU 80 co-exist on RAM 70. A decoding means 90 and a write prohibition means G2 are provided and the writing of CPU 80 is prohibited, whereby the erroneous writing of CPU 80 is prevented.

54/9/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002111429
WPI Acc No: 1979-D1348B/197914
Distributed data processor with master and slave **devices - has** ROM

with internal buses interconnecting data link, resource memory controller and initiator

Patent Assignee: WANG LAB INC (WANG)
Inventor: DUNNING D R; KOPLOW H S; MOROS D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4145739	A	19790320				197914 B

Priority Applications (No Type Date): US 77808112 A 19770620

Abstract (Basic): US 4145739 A

The distributed data-processing system for informational data, comprises a resource memory, a **master device** and one or more **slave** devices. The resource memory has a **ROM** for storing operational instruction data for the system, and on-line storage for storing the informational data.

The **master device** has a **central processor** , a memory, a data link, and a resource memory control unit. Master internal buses interconnect the **master central processor** master memory, master data link and resource memory control unit, and an initiating circuitry.

Title Terms: DISTRIBUTE; DATA; PROCESSOR; MASTER; **SLAVE** ; DEVICE; **ROM** ; INTERNAL; BUS; INTERCONNECT; DATA; LINK; RESOURCE; MEMORY; CONTROL; INITIATE
Derwent Class: T01; T04
International Patent Class (Additional): G06F-003/00; G06F-009/00; **G06F-015/16**
File Segment: EPI
? t54/9/19

54/9/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO

02672763 **Image available**
MULTI-CPU DEVICE

PUB. NO.: 63-289663 [JP 63289663 A]
PUBLISHED: November 28, 1988 (19881128)
INVENTOR(s): MORITA SHINJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-124258 [JP 87124258]
FILED: May 21, 1987 (19870521)
INTL CLASS: [4] **G06F-015/16** ; **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 845, Vol. 13, No. 116, Pg. 37, March 22, 1989 (19890322)

ABSTRACT

PURPOSE: To omit the necessity for providing each CPU with a program **ROM** and to simplify the constitution of a multi-CPU device and the rewriting of a program by storing a **slave** CPU program in a common RAM.

CONSTITUTION: When a **master CPU** 11a in a master module of the multi-CPU device is started, programs for **slave** CPUs 12(sub 1a), 12(sub 2a) stored in a disk 15 are read out and written in a RAM 11c and then the written

programs are read out and written in the common RAM 13. Under said status, the CPU 11a starts the **slave** CPUs 12(sub 1a), 12(sub 2a) and the **slave** CPUs 12(sub 1a), 12(sub 2a) execute the programs written in the common RAM 13. On the other hand, the CPU 11a executes a program written in a **ROM** 11b and respective modules 11, 12(sub 1), 12(sub 2) transfer data through a common bus 14, so that the **ROM** to be used for respective **slave** CPUs 12(sub 1a), 12(sub 2a) can be omitted and the constitution of the device can be simplified.
? t54/9/22,25

54/9/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

02074162 **Image available**
MULTIPROCESSOR SYSTEM

PUB. NO.: 61-288262 [JP 61288262 A]
PUBLISHED: December 18, 1986 (19861218)
INVENTOR(s): YOKOTA MASAYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-129823 [JP 85129823]
FILED: June 17, 1985 (19850617)
INTL CLASS: [4] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 577, Vol. 11, No. 153, Pg. 70, May 19, 1987 (19870519)

ABSTRACT

PURPOSE: To make a **ROM** of a **slave** memory unnecessary to use an overall area as a shared memory by inhibiting start of a **slave** processor until execution of initial program load (IPL) for the **slave** processor is completed.
CONSTITUTION: When a **master processor** 1 is started, a microprogram on a **ROM** m3 as a master memory is started to execute IPL of an IPL program for **slave** processors (1)12 and (n)17 to a RAM m2, and the **master processor** 1 executes this program. Thus, pertinent processing programs are initially loaded to **slave** memories RAM (1)13 and (n)18 from an auxiliary storage device 10. Thereafter, the **master processor** changes the signal from a control circuit 31 to the permission state, and the **slave** processor whose start is permitted starts the program processing on the **slave** memory.

54/9/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

01239361 **Image available**
STARTING CIRCUIT OF MULTI-PROCESSOR SYSTEM

PUB. NO.: 58-176761 [JP 58176761 A]
PUBLISHED: October 17, 1983 (19831017)
INVENTOR(s): SHIGENAGA YOSHIKI
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-059786 [JP 8259786]
FILED: April 12, 1982 (19820412)
INTL CLASS: [3] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)

JOURNAL: Section: P, Section No. 250, Vol. 08, No. 18, Pg. 93, January 26, 1984 (19840126)

ABSTRACT

PURPOSE: To improve the using efficiency of a memory, by storing the starting programs of both a **master processor** and a **slave** processor to an **ROM** for **slave** processor.

CONSTITUTION: When a multi-processor system is started, an address selector 7 switches an address bus AB3 to a **slave** CPU2 and transfers the data of an initial program load IPL for **master CPU** read out of an ROM8 for **slave** CPU to a main RAM4. In the normal state, the selector 7 switches a bus AB3 to a **slave** CPU1, and the RAM4 is occupied by the CPU1. The ROM8 stores not only the processing program of the CPU2 but the data of IPL to the CPU1. A power- on detecting circuit 9 detects that the processor system is switched on. The detecting signal (d) is kept non-active for a period during which the system is switched on and then the power-on state is stabilized. Thereafter, the signal (d) is activated.

46/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016290176 **Image available**
WPI Acc No: 2004-448071/200442
XRPX Acc No: N04-354391

Portable storage device for use with master and slave computers, has flash memory to store data in device, and slave and master ports, both connecting device to slave and master computers via serial bus interface, respectively

Patent Assignee: YANGZHI SCI & TECHNOLOGY CO LTD (YANG-N); FANG J (FANG-I); LIN H (LINH-I)
Inventor: FANG J; LIN H

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040103163	A1	20040527	US 200265903	A	20021127	200442 B
CN 1503149	A	20040609	CN 2003123483	A	20030509	200460

Priority Applications (No Type Date): US 200265903 A 20021127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040103163	A1		12	G06F-015/16	
CN 1503149	A			G06F-015/16	

Abstract (Basic): US 20040103163 A1

NOVELTY - The device has a flash memory for storing data in the portable storage device. A slave port (60) connects the portable device to a slave computer (64) through a universal serial bus interface. A master port (52) connects the portable storage device to a master computer (62) through the serial bus interface. An expansion port connects an external storage apparatus to the storage device.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of connecting a portable storage device to a master computer and a slave computer through a serial bus interface.

USE - Used for connecting a master computer and a slave computer through a serial bus interface (claimed).

ADVANTAGE - The device is capable of providing the master computer to access the data located on the portable storage device and the slave computer, while at the same time preventing the slave computer to access data either on the device or the master computer.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a disk extender.

Master port (52)
Expansion slot (58)
Slave port (60)
Master computer (62)
Slave computer (64)
pp; 12 DwgNo 3/7

Technology Focus:

TECHNOLOGY FOCUS - INDUSTRIAL STANDARDS - The universal serial bus is an IEEE 1394 interface.

Title Terms: PORTABLE; STORAGE; DEVICE; MASTER; SLAVE; COMPUTER; FLASH; MEMORY; STORAGE; DATA; DEVICE; SLAVE; MASTER; PORT; CONNECT; DEVICE; SLAVE; MASTER; COMPUTER; SERIAL; BUS; INTERFACE; RESPECTIVE
Derwent Class: T01; U13; U14
International Patent Class (Main): G06F-015/16
International Patent Class (Additional): G06F-013/14
File Segment: EPI

Manual Codes (EPI/S-X): T01-C07C; **T01-H01B3A** ; T01-H07A; **T01-M02D** ;
U13-C04D; **U14-A03B7**

49/9/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012599111 **Image available**
WPI Acc No: 1999-405217/199934
Related WPI Acc No: 1998-348752; 2001-315852; 2002-382905; 2002-681648; 2003-279234; 2004-803763
XRPX Acc No: N99-302042

Firewall protection architecture for computers

Patent Assignee: ELLIS F E (ELLI-I)
Inventor: ELLIS F E
Number of Countries: 085 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9932972	A1	19990701	WO 98US27058	A	19981217	199934	B
AU 9920046	A	19990712	AU 9920046	A	19981217	199950	
EP 1040418	A1	20001004	EP 98964803	A	19981217	200050	
			WO 98US27058	A	19981217		
CN 1282427	A	20010131	CN 98812442	A	19981217	200131	
JP 2001527236	W	20011225	WO 98US27058	A	19981217	200204	
			JP 2000525814	A	19981217		
US 20020059392	A1	20020516	US 9631855	P	19961129	200237	
			US 9632207	P	19961202		
			US 9633871	P	19961220		
			US 9766313	P	19971121		
			US 9766415	P	19971124		
			US 97980058	A	19971126		
			WO 97US21812	A	19971128		
			US 9768366	P	19971219		
			US 9886516	P	19980522		
			US 9886588	P	19980522		
			US 9885755	A	19980527		
			US 9886948	P	19980527		
			US 9887587	P	19980601		
			US 9888459	P	19980608		
			US 98213875	A	19981217		
			US 99134552	P	19990517		
			US 99315026	A	19990520		
			US 2001884041	A	20010620		
EP 1040418	B1	20030502	EP 98964803	A	19981217	200330	
			WO 98US27058	A	19981217		
DE 69814156	E	20030605	DE 98614156	A	19981217	200345	
			EP 98964803	A	19981217		
			WO 98US27058	A	19981217		
US 20040073603	A1	20040415	US 9631855	P	19961129	200426	
			US 9632207	P	19961202		
			US 9633871	P	19961220		
			US 9766313	P	19971121		
			US 9766415	P	19971124		
			US 97980058	A	19971126		
			WO 97US21812	A	19971128		
			US 9768366	P	19971219		
			US 98213875	A	19981217		
			US 2003663911	A	20030917		

Priority Applications (No Type Date): US 9768366 P 19971219; US 9631855 P 19961129; US 9632207 P 19961202; US 9633871 P 19961220; US 9766313 P 19971121; US 9766415 P 19971124; US 97980058 A 19971126; WO 97US21812 A 19971128; US 9886516 P 19980522; US 9886588 P 19980522; US 9885755 A

19980527; US 9886948 P 19980527; US 9887587 P 19980601; US 9888459 P 19980608; US 98213875 A 19981217; US 99134552 P 19990517; US 99315026 A 19990520; US 2001884041 A 20010620; US 2003663911 A 20030917

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9932972	A1	E	68	G06F-011/00	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9920046	A				Based on patent WO 9932972
EP 1040418	A1	E		G06F-011/00	Based on patent WO 9932972
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
CN 1282427	A			G06F-011/00	
JP 2001527236	W		76	G06F-015/16	Based on patent WO 9932972
US 20020059392	A1			G06F-015/16	Provisional application US 9631855 Provisional application US 9632207 Provisional application US 9633871 Provisional application US 9766313 Provisional application US 9766415 CIP of application US 97980058 CIP of application WO 97US21812 Provisional application US 9768366 Provisional application US 9886516 Provisional application US 9886588 CIP of application US 9885755 Provisional application US 9886948 Provisional application US 9887587 Provisional application US 9888459 Cont of application US 98213875 Provisional application US 99134552 Cont of application US 99315026
EP 1040418	B1	E		G06F-011/00	Based on patent WO 9932972
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
DE 69814156	E			G06F-011/00	Based on patent EP 1040418 Based on patent WO 9932972
US 20040073603	A1			G06F-015/16	Provisional application US 9631855 Provisional application US 9632207 Provisional application US 9633871 Provisional application US 9766313 Provisional application US 9766415 CIP of application US 97980058 CIP of application WO 97US21812 Provisional application US 9768366 Cont of application US 98213875

Abstract (Basic): WO 9932972 A1

NOVELTY - System comprises a computer with controller and microprocessor, and a firewall for PCs limiting access by the network to only some of the hardware, software, firmware etc. The firewall will not permit access by the network to the controller but does allow access to a **slave** microprocessor.

USE - System is for computer networks with PCs or network computers such as servers with microprocessors linked by broadband transmission e.g. the Internet, multitasking and parallel processing.

ADVANTAGE - System avoids excessive idleness of PCs by enabling external parallel processing through the WWW, providing a thousand-fold increase in computer power available to every PC user.

DESCRIPTION OF DRAWING(S) - The drawing shows a simplified diagram of a section of e.g. the Internet with

typical PC (1)
master microprocessor (30)
slave microprocessors (40)
hard drive (61)
floppy diskette (62)
CD- **ROM** (63)
DVD (64)
flash memory (65)
RAM (66)
video display (67)
graphics card (68)
sound card (69)
firewall (50)
pp; 68 DwgNo 10a/15

Title Terms: FIREWALL; PROTECT; ARCHITECTURE; COMPUTER
Derwent Class: T01; W01
International Patent Class (Main): G06F-011/00; **G06F-015/16**
International Patent Class (Additional): G06F-012/14; G06F-013/00; H04L-029/06
File Segment: EPI
Manual Codes (EPI/S-X): T01-H01C2; T01-H07C5E; T01-J12C; **T01-M02D** ; W01-A05B; W01-A06B5; W01-A06B7

49/9/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009757041 **Image available**
WPI Acc No: 1994-036892/199405
XRPX Acc No: N94-028714

Programmable microprocessor with booting technique for slave processors - uses FIFO memory to connect host **computer bus and slave microprocessor memory bus**

Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: ENDSLEY J A
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 581698	A1	19940202	EP 93420315	A	19930723	199405	B
CA 2097874	A	19940129	CA 2097874	A	19930607	199415	
CA 2097874	C	19980825	CA 2097874	A	19930607	199845	
US 6438683	B1	20020820	US 92922116	A	19920728	200257	

Priority Applications (No Type Date): US 92922116 A 19920728
Cited Patents: 02Jnl.Ref; EP 262468; EP 268285
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 581698	A1	E	8	G06F-009/44	
Designated States (Regional): DE FR GB					
CA 2097874	A			G06F-012/08	
CA 2097874	C			G06F-012/08	
US 6438683	B1			G06F-009/445	

Abstract (Basic): EP 581698 A

The computer system includes a **host** computer, a programmable microprocessor (the slave processor) controlled by the **host** computer, a FIFO memory connected between the **host** computer and the microprocessor and means for providing a boot programme and/or boot data from the **host** computer to the microprocessor through the FIFO memory.

When the boot programme functions, operating instructions for the microprocessor are read into the microprocessor's own random access memory. The FIFO memory may be **unidirectional** or bidirectional.

ADVANTAGE - Avoids inconvenience associated with providing slave processor with its own boot **ROM** or the bulk and cost of dual ported RAM and offers greater speed of communication than dual ported RAM.

Dwg.1/3

Title Terms: PROGRAM; MICROPROCESSOR; TECHNIQUE; SLAVE; PROCESSOR; FIFO; MEMORY; CONNECT; **HOST** ; COMPUTER; BUS; SLAVE; MICROPROCESSOR; MEMORY; BUS

Derwent Class: T01

International Patent Class (Main): G06F-009/44; G06F-009/445; G06F-012/08

International Patent Class (Additional): G06F-005/06

File Segment: EPI

Manual Codes (EPI/S-X): T01-F05B; T01-H03D; T01-M02

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